In The Claims

1. (Currently Amended) A processor readable medium, which is physical, encoding a data structure for supporting one or more packet modification operations, the data structure comprising:

a first pointer to a sequence of one or more commands, ~~for execution~~executable by a processor, implementing one or more packet modification operations and stored in a first memory area; and

a second pointer to a burst of one or more data or mask items, stored in a second memory area distinct from the first, for use by the processor in executing the one or more commands ~~stored in a second memory area distinct from the first~~;

~~wherein the data structure is located in a third memory and the data structure is accessed via a data structure index, wherein the data structure index is embedded in the one or more packets;~~

wherein at least one command in the sequence implements a packet modification operation that uses at least one of the one or more data or mask items to modify a packet~~data is selectively shifted and masked in each of plurality of categories responsive to one or more decoded commands, thereby performing one or more packet modification operations in the packet;~~

~~wherein the selectively shifted and masked data is logically summed into the plurality of categories~~.

2. (Currently Amended) The processor readable medium of claim 1 wherein ~~the data structure is generated during receive-side classifications processing of a packet~~the first and second memory areas are located in different memories.

3. (Currently Amended) The processor readable medium of claim 1 wherein ~~the data structure is generated by a host CPU coupled to a switch fabric~~the first and second memory areas are located in the same memory.

4. (Original) The processor readable medium of claim 1 wherein the one or more commands are stored in a packed format.

5. (Original) The processor readable medium of claim 1 wherein the one or more data or mask items are stored in a packed format.

6. (Original) The processor readable medium of claim 1 wherein the one or more data or mask items comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.

7. (Currently Amended) The processor readable medium of claim 1 wherein the first and second memory areas are located in a memory implemented off chip ~~from a modification~~in relation to the processor ~~configured to execute the one or more commands~~.

8. (Currently Amended) The processor readable medium of claim 1 wherein the first memory area is located in a memory implemented on chip ~~with the modification~~in relation to the processor.

9. (Original) The processor readable medium of claim 1 wherein the data structure comprises one or more pointers, each to a sequence of one or more commands implementing one or more packet modification operations.

10. (Original) The processor readable medium of claim 9 wherein the data structure comprises one or more pointers, each to a burst of one or more data or mask items.

11. (Currently Amended) A method of performing one or more packet modification operations on a packet associated with a data structure link, the method comprising:

~~performing packet classification while the packet is located within a first portion of a switch;~~

~~inserting a data structure index in the packet while the packet is located within a second portion of the switch;~~

retrieving from a memory a data structure corresponding to the data structure ~~index~~link, ~~and~~ the data structure comprising ~~first~~ a first pointer to a sequence of one or

more commands, for execution by a processor, implementing one or more packet modification operations and stored in a first memory area, and a second pointer to a burst of one or more data or mask items, stored in a second memory area distinct from the first, for use by the processor in executing the one or more commands ~~stored in a second memory area distinct from the first~~;

retrieving from the first memory area the one or more commands;

retrieving from the second memory area the one or more data or mask items ~~for use by the one or more commands~~; and

executing the one or more commands by the processor, thereby performing one or more packet modification operations on the packet;

~~wherein the data structure is located in a third memory and the data structure is accessed via a data structure index, wherein the data structure index is embedded in the one or more packets;~~

wherein at least one of the one or more commands retrieved from the first memory area implements a packet modification operation that uses at least one of the one or more data or mask items to modify the packet~~data is selectively shifted and masked in each of plurality of categories responsive to one or more decoded commands, thereby performing one or more packet modification operations in the packet;~~

~~wherein the selectively shifted and masked data is logically summed into the plurality of categories~~.

12. (Currently Amended) The method of claim 11 wherein ~~the first portion of the switch is an egress portion of the switch~~a switch associates the data structure link with the packet.

13. (Currently Amended) The method of claim [[11]]12 wherein the switch associates the data structure link with the packet by inserting a data structure index corresponding to the link into a header of the packet~~second portion of the switch is an ingress portion of the switch~~.

14. (Currently Amended) The method of claim [[12]]11 wherein the first and second

memory areas are located in different memories~~the data structure is generated during receive side classifications processing of a packet~~.

15. (Currently Amended) The method of claim [[12]]11 wherein the first and second memory areas are located in the same memory~~data structure is generated by a host CPU coupled to a switch fabric~~.

16. (Currently Amended) The method of claim [[12]]11 wherein the one or more commands are stored in a packed format.

17. (Currently Amended) The method of claim [[12]]11 wherein the one or more data or mask items are stored in a packed format.

18. (Currently Amended) The method of claim [[12]]11 wherein the one or more data or mask items comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.

19. (Currently Amended) The method of claim [[12]]11 wherein the first and second memory areas are located in a memory implemented off chip ~~from a modification~~ in relation to the processor ~~which executes the one or more commands~~.

20. (Currently Amended) The method of claim [[12]]11 wherein the first memory area is located in a memory implemented on chip ~~with the modification~~ in relation to the processor.

21. (Original) The method of claim 12 wherein the data structure comprises one or more pointers, each to a sequence of one or more commands implementing one or more packet modification operations.

22. (Original) The method of claim 12 wherein the data structure comprises one or more pointers, each to a burst of one or more data or mask items.

23. (Canceled)

24. (Previously Presented) A ~~pipeline processor core~~packet modification system comprising:

a memory storing a data structure comprising ~~two or more pointers~~a first pointer to a sequence of one or more commands implementing one or more packet modification operations and stored in a first memory area; and a second pointer to a burst of one or more data or mask items, stored in a second memory area distinct from the first, for use in the one or more packet modification operations; and

a processor configured to retrieve and execute the one or more commands pointed to by the first pointer, wherein at least one of the one or more commands implements a packet modification operation that uses at least one of the one or more data or mask items to modify a packet.

~~a command fetch stage configured to fetch one or more commands obtained using a first pointer to access a first memory;~~

~~a command decode stage configured to decode the one or more commands;~~

~~an address and mask generation stage configured to generate one or more addresses and one or more mask for each of the commands;~~

~~a data shift, mask and sum stage wherein packet data is selectively shifted and masked in each of plurality of categories in response to a decoded command, wherein data shifting and masking is based upon a burst of one or more data and mask items obtained using a second pointer to access a second memory which is distinct from the first memory;~~

~~wherein the pipeline processor core supports a data structure comprising two or more pointers;~~

~~wherein the first and second pointers are located in the data structure that is accessed from a third memory via a data structure index, wherein the data structure index is embedded in one or more data packets;~~

~~wherein the selectively shifted and masked data is logically summed into the plurality of categories.~~

25.-27. (Canceled)

28. (New) The system of claim 27 wherein the first and second memory areas are located in different memories.

29. (New) The system of claim 27 wherein the first and second memory areas are located in the same memory.

30. (New) The system of claim 27 wherein the packet modification processor comprises a pipeline processor core configured to retrieve the one or more commands in a first stage, and execute the one or more commands in one or more subsequent stages.